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Linkedin Page : https://www.linkedin.com/company/vlsifrontend

1. Common Websites

1. https://verificationguide.com/
2. http://www.testbench.in/
3. https://www.chipverify.com/
4. http://www.asic-world.com/
5. https://verificationacademy.com/
6. Synopsys UVM
7. Easier UVM
8. Digital Electronics

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2. DIGITAL DESIGN

1. Digital Electronics by Neso Academy
2. Digital Design Morris Mano
3. Digital Design by NPTEL.
4. Digital Design Widmer Tocci
5. http://www.fullchipdesign.com/
6. Digital Design Course
7. Electronics Hub
8. Priority Encoder

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3. VHDL

1. VHDL Basics
2. VHDL Merged
3. VHDL Package and Other Constructs
4. VHDL by Intel
5. VHDL Mini Reference
6. Intel FPGA Official Youtube Link
7. HDL Works
8. ASIC World Webisite
9. VHDL Tutorial
10. FPGA Design using VHDL Lectures
11. VHDL Attributes
12. Golden Reference Guide
13. VHDL Primer
14. Tutorials Point VHDL

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4. Verilog

1. Digital System Design with VHDL
2. Chip Verify
3. Verilog Quick Reference
4. Verilog By Intel
5. Full Adder
6. Verilog Examples
7. Verification Guide
8. Intel FPGA Official Youtube Link
9. RTL Design
10. Verilog by NPTEL
11. Golden Reference Guide Verilog
12. Golden Reference Guide SV
13. Verilog
14. HDL Works
15. Verilog code for FIFO memory
16. Testbench_in
17. Verilog Tips and Tricks/File Reading
18. Asic World
19. RF Wireless World
20. Full Chip Design
21. Fpga4fun
22. Only Vlsi
23. Verilog
24. Intro to Verilog
25. FSM by Berkeley EDU
26. System Verilog For Design Quick Reference

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5. System Verilog

1. Verification Guide SV
2. System Verilog basic PPT
3. SV by Cadence
4. SV Interfaces
5. Operators
6. Operators
7. Verification Excellence SV and UVM
8. Testbench_in
9. System Verilog for Verification
10. Static Variables and functions
11. Static and Automatic Lifetime of Variable and Methods
12. DVCON_2020
13. Verification academy Events
14. casting string to enum
15. casting string to enum
16. The Art Of Verification
17. VLSI Verify
18. always block in task
19. Amiq Consulting

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6. Fork- Join Questions

1. https://verificationacademy.com/forums/systemverilog/fork-within-loop-join-all
2. https://verificationacademy.com/forums/systemverilog/loop-inside-fork-joinnone
3. https://verificationacademy.com/forums/systemverilog/fork-joinnone-inside-loop#reply-38644
4. https://verificationacademy.com/forums/systemverilog/controlling-fork-joinnone-threads-execution
5. https://verificationacademy.com/forums/systemverilog/controlling-fork-joinnone-threads-execution
6. https://verificationacademy.com/forums/systemverilog/automatic-variables-fork
7. https://testbench4u.com/2018/10/01/fork-join-tricky-example/
8. https://dvtalk.me/2020/12/06/about-systemverilog-process-and-fork/
9. https://blog.verificationgentleman.com/2014/03/10/a-subtle-gotcha-when-using-forkjoin.html

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7. Universal Verification Methodology (UVM)

1. UVM Class Reference
2. UVM by Synopsys
3. Easier UVM By John Aynsley
4. Verification Guide UVM
5. Chip verify UVM
6. Mentor Graphics Verification Academy UVM
7. UVM Configuration Data Base DVCON
8. Golden Reference Guide UVM
9. Learn UVM Verification
10. UVM TEST NAME
11. UVM command line processor
12. Mentor UVM Cook Book
13. UVM Doulos
14. Test bench UVM
15. UVM for Beginners
16. UVM Primer
17. Verilab UVM
18. UVM TLM Interfaces
19. uvm_re_match
20. UVM Coding
21. UVM Commandline Argument
22. UVM Verbosity
23. http://cluelogic.com/category/uvm/
24. https://blog.verificationgentleman.com/years/
25. UVM Event
26. https://www.amiq.com/consulting/2014/08/08/how-to-stop-the-simulation-on-uvm_error/ -- UVM ERROR
27. https://www.vlsiguru.com/uvm-notes2020/ -- UVM Notes VLSIGURU
28. UVM Tips & Tricks
29. https://vlsiverify.com/
30. https://www.amiq.com/consulting/resources/

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31. uvm_re_match
32. Verilab UVM

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8. PROTOCOLS ::(AXI/SPI/I2C/UART/AXI4/AXI STREAM etc...)

SPI Protocol:

1. https://electrosome.com/spi/
2. http://pythonway-pw.blogspot.com/2017/05/spi-working-with-verilog-code_99.html
3. https://learn.sparkfun.com/tutorials/serial-peripheral-interface-spi/all
4. https://www.youtube.com/watch?v=AuhFr88mjt0

APB Protocol:

1. https://youtu.be/BfBnlZuQHTs
2. https://youtu.be/ZQa8DIJfa2s

AXI Protocol:

1. AXI Part 1 : https://youtu.be/i1vzrANrsOc
2. AXI Part 2 : https://youtu.be/cZvO_vGNQq8
3. AXI Part 3 : https://youtu.be/LkeR5UG10tc
4. http://www.gstitt.ece.ufl.edu/courses/fall15/eel4720_5721/labs/refs/AXI4_specification.pdf -- AXI Spec
5. https://www.xilinx.com/support/documentation/ip_documentation/axi_interconnect/v2_1/pg059-axi-interconnect.pdf -- AXI Interconnect
6. https://www.xilinx.com/support/documentation/ip_documentation/axi_ref_guide/latest/ug761_axi_reference_guide.pdf --AXI

AHB Protocol:

1. AHB Part 1 : https://youtu.be/bEF8eXZZt7k
2. AHB Part 2 : https://youtu.be/Pkv4tVlsfiA
3. AHB Part 3 : https://youtu.be/jpugXK8srgs

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Other Links:

1. http://pythonway-pw.blogspot.com/2018/02/i2c-verilog-code-and-working.html -- I2C
2. http://infocenter.arm.com/help/index.jsp --Arm Official Website
3. https://www.ti.com/lit/ds/symlink/tlk100.pdf?ts=1590932876482 -- Ethernet PHY
4. http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.set.amba/index.html --Arm Official Website
5. http://verificationexcellence.in/soc-bus-protocols/ -- Bus Protocols.
6. https://courses.cs.washington.edu/courses/cse466/12au/calendar/07-Communication-posted.pdf – Basics Of Communication.
7. https://www.doulos.com/knowhow/verilog_designers_guide/models/universal_asynchronous_receiver_uar/
8. http://www.cpri.info/downloads/CPRI_v_7_0_2015-10-09.pdf -- CPRI
9. http://www.cpri.info/downloads/eCPRI_v_1_1_2018_01_10.pdf -- eCPRI
10. ETHERNET PHY https://youtu.be/JH3cMYErmKI
11. https://blogs.synopsys.com/vip-central/2019/11/21/demystifying-pcie-pipe-5-1-serdes-architecture/ -- PCIE Serdes.

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9. Coverage

- https://www.amiq.com/consulting/2015/09/18/functional-coverage-patterns-bitwise-coverage/
- https://www.amiq.com/consulting/2015/09/18/functional-coverage-patterns-bitwise-coverage/#bit_masking_coverage
- https://www.amiq.com/consulting/blog/page/3/?tag=functional-coverage
- https://www.amiq.com/consulting/2018/01/15/how-to-alternative-ways-to-implement-bitwise-coverage/
- https://www.amiq.com/consulting/2014/09/17/how-to-ignore-cross-coverage-bins-using-expressions-in-systemverilog/
- https://verificationguide.com/systemverilog/systemverilog-functional-coverage/
- http://www.testbench.in/CO_00_INDEX.html
- https://verificationacademy.com/forums/coverage/coverage-any-one-bits-register

Parameterized Interfaces and Reusable VIP

- https://blogs.synopsys.com/vip-central/2015/01/27/parameterized-interfaces-and-reusable-vip-part-1/
- https://blogs.synopsys.com/vip-central/2015/02/19/parameterized-interfaces-and-reusable-vip-part-2/
- https://blogs.synopsys.com/vip-central/2015/02/24/parameterized-interfaces-and-reusable-vip-part-3/

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10. SCRIPTING ::(Perl/Shell/Python/Makefile/Bash/Awk, Tcl)

UNIX/LINUX:

https://ivlsi.com/basic-linux-commands-vlsi/

PERL:

1. https://www.youtube.com/user/madhurbhatia89/playlists

SHELL:

2. https://www.youtube.com/user/madhurbhatia89/playlists
3. https://www.youtube.com/playlist?list=PLS1QulWo1RIYmaxcEqw5JhK3b-6rgdWO_
4. https://www.youtube.com/playlist?list=PL2qzCKTbjutJRM7K_hhNyvf8sfGCLklXw
5. https://www.youtube.com/playlist?list=PL8cE5Nxf6M6b8qW7CSMsdKbEsPdG9pWfu
6. https://gutl.jovenclub.cu/wp-content/uploads/2013/10/Linux.Shell_.Scripting.Cookbook.pdf

PYTHON:

1. https://www.w3schools.com/python/default.asp
2. https://www.tutorialspoint.com/python/
3. https://realpython.com/python-first-steps/
4. https://www.javatpoint.com/python-tutorial
5. https://www.youtube.com/user/madhurbhatia89/playlists

TCL:

1. https://wiki.tcl-lang.org/page/Tcl+Tutorial+Lesson+0
2. https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/manual/tclscriptrefmnl.pdf
3. https://www.youtube.com/playlist?list=PL1h5a0eaDD3rsGDFnVki_fFEtDWQfXjca

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Makefile:

1. https://www.youtube.com/playlist?list=PLbMVogVj5nJRa3VKt_eyZdJ_DitCz1cvQ -- Linux,tcl,perl,Makefile by nptel.
2. https://www.tldp.org/LDP/Bash-Beginners-Guide/Bash-Beginners-Guide.pdf -- Bash Guide for Beginners.
3. https://www.gnu.org/software/make/manual/html_node/#toc-Overview-of-make --GNU Makefile.
4. https://www.gnu.org/software/make/manual/html_node/Introduction.html#Introduction -- GNU Makefile.https://www.gnu.org/software/make/manual/html_node/Rule-Introduction.html#Rule-Introduction --GNU Makefile.
5. https://www.gnu.org/software/make/manual/html_node/Phony-Targets.html#Phony-Targets --GNU Makefile.
6. https://www.gnu.org/software/make/manual/html_node/Conditional-Example.html --GNU Makefile.
7. https://www.gnu.org/software/make/manual/html_node/Conditional-Example.html --GNU Makefile.
8. http://www.asic-world.com/
9. http://www.asicguru.com/

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11. TIMING ANALYSIS, STA & CDC

1. https://www.eng.biu.ac.il/temanad/digital-vlsi-design/ --Timing Analysis
2. http://www.eng.biu.ac.il/temanad/files/2017/02/Lecture-3-STA.pdf --Timing Analysis.
3. https://youtube.com/playlist?list=PLpCkjM331Aa8JNoZ1s1o1txve2wlf9pCP -- Static Timing Analysis ,Yash Jain
4. https://www.youtube.com/watch?v=RTcZOl2e8PI&feature=youtu.be – CDC Intel
5. https://www.youtube.com/watch?v=HMAqjjCuDEI – Setup and Hold Slack, Intel
6. https://www.youtube.com/watch?v=6D-w8mOttnE&feature=youtu.be – Timing Analysis , Intel
7. https://vlsiuniverse.blogspot.com/2016/12/setup-hold-interview-questions.html
8. http://www.vlsi-expert.com/ -- VLSI Expert, STA.
9. https://www.eetimes.com/understanding-clock-domain-crossing-issues/# --CDC Explained.
10. https://www.edn.com/basics-of-multi-cycle-false-paths/ -- Multicycle and false paths EDN.
11. https://www.edn.com/synchronizer-techniques-for-multi-clock-domain-socs-fpgas/ -- Synchronization Techniques.
12. http://www.ee.bgu.ac.il/~digivlsi/slides/STA_9_1.pdf --STA
13. http://www.ee.bgu.ac.il/~digivlsi/slides/synopsys_class_3_6_1.pdf --STA
14. https://www.ijitee.org/wp-content/uploads/papers/v8i7s/G10240587S19.pdf --STA International Journal.
15. https://classes.engineering.wustl.edu/ese461/ -- Timing Analysis, Design Automation for Integrated Circuit systems.
16. https://www.youtube.com/c/TeamVLSI/videos
17. https://www.youtube.com/watch?v=UGGkKZylJBo – Timing closure, Intel
18. https://www.youtube.com/c/TechnicalBytes/playlists
19. http://www.sunburst-design.com/papers/CummingsSNUG2008Boston_CDC.pdf
20. https://classes.engineering.wustl.edu/ese461/Lecture/week7b.pdf -- Timing Analysis
21. Link(Verilog, VHDL, Timing, Quartus Prime Software, Qsys Editor, Platform Deisgner etc).
22. https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an584.pdf -- Timing Closure Methodology for Advanced FPGA Designs

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23. https://vlsiuniverse.blogspot.com/search/label/How%20to%20avoid%20setup%20and%20hold%20time%20violations -STA & Timing
24. https://www.allaboutcircuits.com/technical-articles/why-how-pipelining-in-fpga/ --What is pipelining.
25. https://www.youtube.com/watch?v=A3gLtielLvc
26. https://youtu.be/2V41i4xVTZ8 -- Setup , hold , propagation delay , timing errors , Metastability.
27. http://www.sunburst-design.com/papers/CummingsSNUG2002SJ_Resets.pdf -- Sunburst Reset Strategy.
28. https://www.youtube.com/watch?v=0Ho4rDswOeE&list=PL0pU5hg9yniZ2ka-XBXROXNR0pAEAEFCB --Intel FPGA Official Youtube

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12. CODING GUIDELINES AND STYLES

1. https://hackaday.io/project/20751-memory-on-cyclone5-fpga/details -- Memory Coding Style.
2. https://inst.eecs.berkeley.edu/~cs150/sp12/resources/FSM.pdf --FSM Code style.
3. https://www.xilinx.com/support/documentation/white_papers/wp231.pdf – HDL coding Practises by XILINX.

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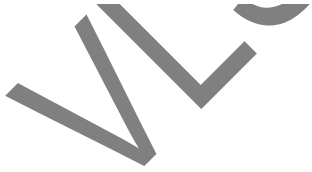
13. Inferring a Latch

1. https://stackoverflow.com/questions/22459413/what-is-inferred-latch-and-how-it-is-created-when-it-is-missing-else-statement-i
2. https://stackoverflow.com/questions/20036401/if-statements-causing-latch-inference-in-verilog
3. https://www.nandland.com/articles/how-to-avoid-transparent-latches-in-vhdl-and-verlog.html
4. http://web.engr.oregonstate.edu/~traylor/ece474/vhdl_lectures/inferring_storge_elements.pdf
5. http://www.doe.carleton.ca/~shams/ELEC3500/Ver2Syn.pdf
6. https://www.edaboard.com/showthread.php?313149-inferring-latch(es)-for-signal-VHDL-error
7. https://www.allaboutcircuits.com/technical-articles/vhdl-incomplete-if-statements-and-latch-inference/
8. https://www.doulos.com/knowhow/fpga/latches/
9. https://www.allaboutcircuits.com/technical-articles/use-of-clock-gating-to-reduce-power-consumption/ -- Clock Gating.
10. https://www.cypress.com/documentation/component-datasheets/edge-detector -- Edge Detector Circuit.
11. https://groups.google.com/forum/#!topic/embeddednewbies/c6bMIbDUnt8 --Sunburst Papers.
12. https://vdocuments.mx/search?q=Synthesizable+SystemVerilog%3A+Busting+the+Myth+that+...+%3F%3FSNUG+Silicon+Valley+2013+3+Synthesizing+SystemVerilog+1.0+Introduction+%E2%80%94+debunking+the+Verilog+vs.+SystemVerilog+myth+There+is+a+common+misconception+that+...&u=1 -- Sunburst Papers.



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14. Aynchronous FIFO's Explained

1. https://hardwaregeeksblog.files.wordpress.com/2016/12/fifodepthcalculationmadeeasy2.pdf -- FIFO Depth Calculation
2. https://zipcpu.com/blog/2018/07/06/afifo.html
3. https://zipcpu.com/blog/2017/10/20/cdc.html
4. https://esrd2014.blogspot.com/p/first-in-first-out-buffer.html
5. http://electrosofts.com/verilog/fifo.html
6. http://www.sunburst-design.com/papers/CummingsSNUG2002SJ_FIFO1.pdf -- Sunburst Asynchronous FIFO.
7. https://github.com/JonathanJing/Asynchronous-FIFO
8. https://www.youtube.com/watch?v=Nr8q5VW-mXI -- FIFO in FPGA.

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15. Interviews & Job Prep

1. Verilog Frequently Asked Questions. https://www.google.com/url?sa=t&source=web&rct=j&url=https://lucc.pl/inf/architektura_komputerow_2/verilog/verilog_faq.pdf&ved=2ahUKEwio-4mn7truAhURX30KHWNhA-EQFjADegQIARAB&usg=AOvVaw3P28hknlasn1cuzeZESTL5
2. https://www.theartofverification.com/
3. https://www.wisdomjobs.com/e-university/universal-verification-methodology-uvm-interview-questions.html --UVM Interview Questions.
4. http://www.asic.co.in/vlsi_presentations.htm
5. https://vlsiuniverse.blogspot.com/2016/12/setup-hold-interview-questions.html
6. https://www.bestsampleresume.com/job-descriptions/engineer/fpga-design-engineer.html
7. http://only-vlsi.blogspot.com/2009/01/digital-design-interview-questions.html
8. https://www.wisdomjobs.com/e-university/verilog-interview-questions.html

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16. FPGA

1. https://www.intel.com/content/www/us/en/programmable/documentation/jbr1444752564689.html#esc1445881961208 --Intel Hyperflex Architecture.
2. https://numato.com/kb-category/getting-started-with-fpga/
3. https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_hp_hb.pdf -- Intel Stratix 10 user guide
4. https://www.xilinx.com/support/documentation/sw_manuals/xilinx11/ise_c_implement_fpga_design.htm -- XILINX FPGA's
5. https://www.youtube.com/watch?v=bwoyQ_RnaiA – FPGA Design by Intel.
6. https://www.embedded.com/model-based-fpga-design-tool-quietly-gains-adherents/
7. https://www.mentor.com/products/fv/multimedia/player/coverage-plan-driven-verification-for-fpgas-4d3ebed0-d534-47f4-ae75-ee290f676593 -- Coverage & Plan-Driven Verification for FPGAs

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17. FPGA Constraints

1. https://www.edn.com/fpga-constraints-for-the-modern-world-product-how-to/ -- FPGA constraints.

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18. Tools

1. https://www.edaplayground.com/ -- EDA Play Ground
2. https://www.youtube.com/watch?v=A1qhavaVlnw How to use www.edaplayground.com EDA by VLSI Guru
3. VIVADO TCL
4. Quartus Prime Tool Tutorial, Clock Fabric Youtube Channel
5. Questasim
6. Quartus Prime Timing Analyzer

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19. Editors

1. https://www.youtube.com/watch?v=NPtLV_hgomI&list=PLY7ywYIJrK2lHa0p_-P42g-ku5B0mns_R&index=1 -- GVIM Usage
2. https://www.youtube.com/watch?v=jXud3JybsG4 -- GVIM
3. http://www.verificationguide.com/p/gvim-or-vim-commands-set.html --- GVIM commands
4. https://www.cs.cmu.edu/~15131/f17/topics/vim/vim-cheatsheet.pdf -- GVIM cheat sheet
5. https://vim.rtorr.com/
6. https://devhints.io/vim
7. http://www.atmos.albany.edu/daes/atmclasses/atm350/vi_cheat_sheet.pdf
8. https://rumorscity.com/2014/08/16/5-best-vim-cheat-sheet/
9. https://www.cs.oberlin.edu/~kuperman/help/vim/windows.html
10. https://www.ele.uri.edu/faculty/vetter/Other-stuff/vi/vimtips.html
11. https://vim.fandom.com/wiki/Moving_lines_up_or_down
12. https://learninggentleman.com/programming/in-these-series-i-share-some-of-my-favorite-vim-editor-tips/

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20. Cron Job

- https://sagar5258.blogspot.com/2015/04/crontab-in-linux-cron-jobscheduled-task.html

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21. Other

1. http://www.sunburst-design.com/ --Sunburst Design Official Website.
2. https://www.verilogpro.com/systemverilog-always_comb-always_ff/-- Verilog pro Website
3. https://hdvacademy.blogspot.com/p/index.html?view=classic -- Hardware Design and Verification Academy.
4. https://www.embedded.com/model-based-fpga-design-tool-quietly-gains-adherents/
5. http://verificationexcellence.in/ -- Verification Excellence Official Website.
6. https://www.chipverify.com/ -- Chip Verify Official Website.
7. http://blog.imm.cnr.it/content/linux-check-disk-space-command-view-system-disk-usage-df-and-du -- Disk Space Usage.

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22. GIT

1. https://dont-be-afraid-to-commit.readthedocs.io/en/latest/git/index.html

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23. NPTEL Useful Courses

1. https://nptel.ac.in/courses/117/105/117105080/
2. https://nptel.ac.in/courses/106/105/106105185/
3. https://nptel.ac.in/courses/106/105/106105165/
4. https://nptel.ac.in/courses/106/103/106103016/
5. https://nptel.ac.in/courses/106/103/106103116/
6. https://nptel.ac.in/courses/117/108/117108040/
7. https://nptel.ac.in/courses/117/106/117106092/
8. https://nptel.ac.in/courses/117/106/117106086/
9. https://nptel.ac.in/courses/108/106/108106137/

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24. 5G

1. https://www.keysight.com/upload/cmc_upload/All/Understanding_the_5G_NR_Physical_Layer.pdf -- Understanding 5G Layers.
2. https://www.youtube.com/watch?v=RagHojSWEz8&list=PLfUa5X9whlE9Ul3j1PcZ5FUKFsVixjiXP&index=1 --5G